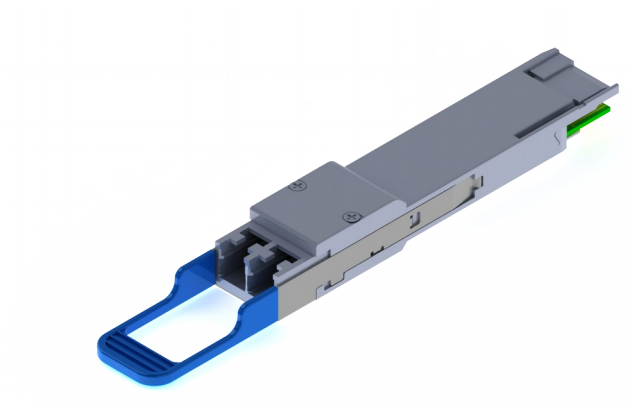
WAVESPLITTER™ TECHNOLOGIES, INC.

Data Sheet

200-Gbps QSFP-DD 2xCWDM4 Optical Transceiver
P/N: WST-QD2H-2CM4-C



Features:

- Electrical and Optical specifications followed by CAUI-4 and 100G CWDM4 MSA, respectively.
- QSFP-DD compliant to MSA of QSFP-DD Rev. 2.0
- Up to 2km link length over single mode fiber at 200Gbps
- Duplex CS Connectors as optical interface
- Low power consumption of Max. 7W
- Hot pluggable electrical interface
- I²C Management Interface with clock rate up to 400KHz
- 0 to 70°C case temperature operating range
- RoHS-6 Compliant (lead-free)

Applications:

- 2x100GBASE-CWDM4 Ethernet links
- HPC Interconnects
- Proprietary Interconnections

Absolute Maximum Rating

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Parameter	Min	Max	Unit	Note
Storage Temperature	-40	85	℃	
3.3V Power Supply Voltage	-0.3	3.6	V	
Data Input Voltage- Single Ended	-0.3	V_{cc}+0.3	V	
Control Input Voltage	-0.3	3.6	V	
Relative Humidity	5	85	%	1

Notes:

1. Non-condensing.

Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Note
Case Operating Temperature	0		70	℃	
Power Supply Voltage	3.135	3.3	3.465	V	
Date Rate per Channel		25.78125		Gbps	
Bit Error Ratio		10^{-12}			
Control Input Voltage High	2.6		Vcc+0.3	V	
Control Input Voltage Low			0.6	V	
Two Wire Serial (TWS) Interface Clock Rate		100	400	kHz	
Differential Data Input / Output Load		100		Ohms	
Link Reach			2	km	

Electrical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transceiver Electrical Characteristics						
TRx Power Consumption				7	W	
Transmitter Electrical Characteristics						
Data Input Differential Peak-to-Peak Voltage Swing	ΔVDI PP			900	mVpp	
Common Mode Voltage (Max)				1.9	V	
Common Mode Voltage (Min)		0			V	
Differential Input Return Loss		9.5-0.37f, 0.01<=f<8 GHz, 4.75 – 7.4Log$_{10}$(f/14), 8<=f<19 GHz			dB	
Differential to common mode input return loss		22-20(f/25.78), 0.01<=f<12.89 GHz, 15-6(f/25.78), 12.89<=f<19 GHz				
Receiver Electrical Characteristics						
Differential Output Return Loss		9.5-0.37f, 0.1<=f<8 GHz, 4.75 – 7.4Log$_{10}$(f/14), 8<=f<19 GHz			dB	
Differential to common mode output return loss		22-20(f/25.78), 0.01<=f<12.89 GHz, 15-6(f/25.78), 12.89<=f<19 GHz			dB	

Differential Output Voltage				900	mV	WST-QSFP+LR4L-C
Eye Width		0.57			UI	
Eye Height, Differential		228			mV	

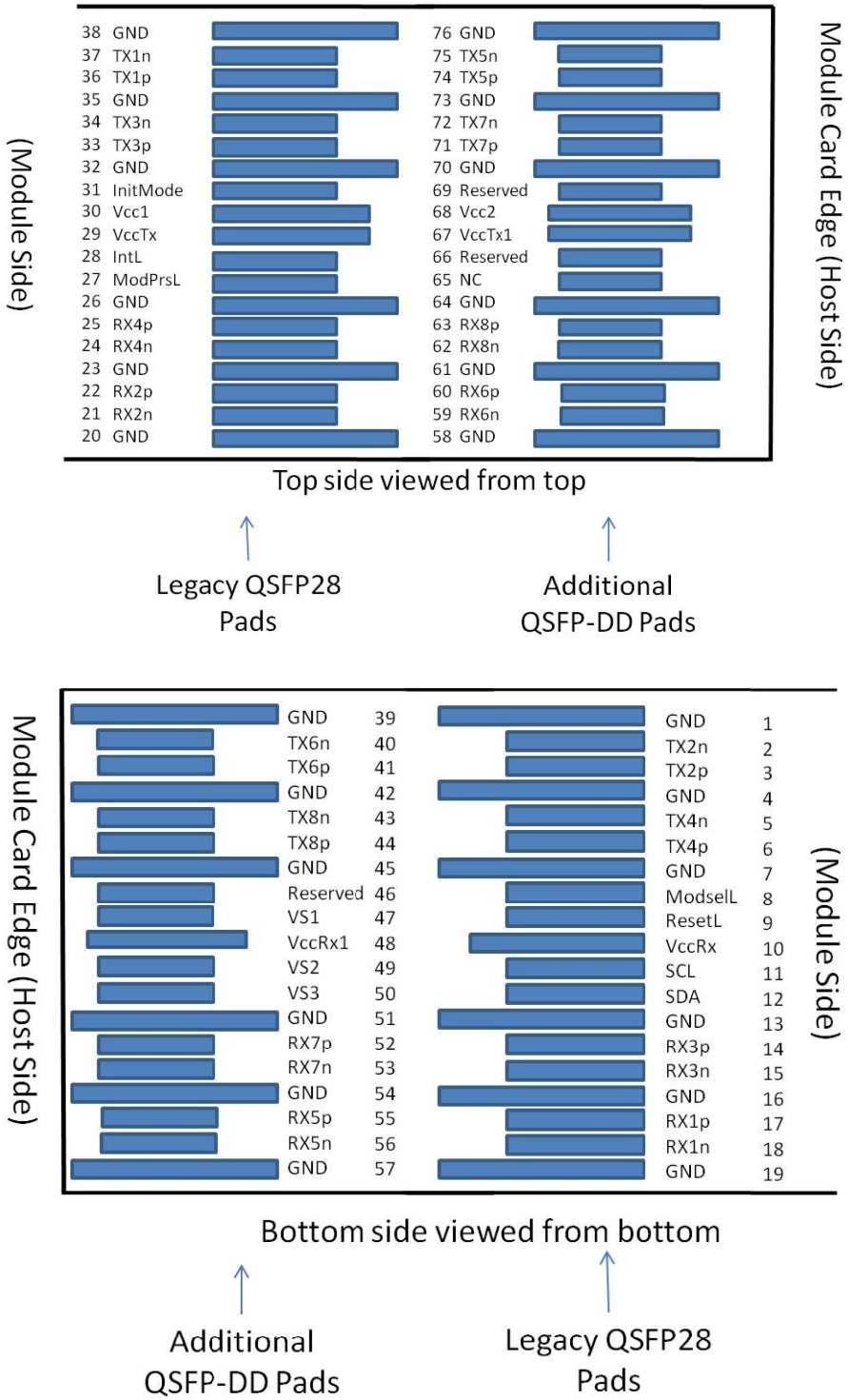
Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter Optical Characteristics						
Lane Center Wavelengths (Range)	Ch0	1264.5 – 1277.5			nm	
	Ch1	1284.5 – 1297.5				
	Ch2	1304.5 – 1317.5				
	Ch3	1324.5 – 1337.5				
Side-Mode Suppression Ratio	SMSR	30			dB	
Output Optical Power: Average	PO AVE	-6.5		2.5	dBm	
Output Optical Modulation Amplitude, per Lane	OMA	-4		2.5	dBm	1
Extinction Ratio	ER	3.5			dB	
Transmitter Eye Mask		0			%	2
Receiver Optical Characteristics						
Lane Center Wavelengths (Range)	Ch0	1264.5 – 1277.5			nm	
	Ch1	1284.5 – 1297.5				
	Ch2	1304.5 – 1317.5				
	Ch3	1324.5 – 1337.5				
Damage Threshold		3.5			dBm	
Average receive power, Each Lane		-11.5		2.5	dBm	3
Optical Modulation Amplitude (OMA)				2.5	dBm	
Non-stressed Receiver Sensitivity in OMA				-10	dBm	4
Receiver Reflectance				-26	dB	

Notes:

1. TDP value and dependent parameters are subject to confirmation.
2. Transmitter eye mask is defined by 100G-CWDM4 Specification 1.1.
3. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.
4. Measured with conformance test signal at TP3 for BER = $5x10^{-5}$

QSFP-DD Module Pad Assignments and Descriptions



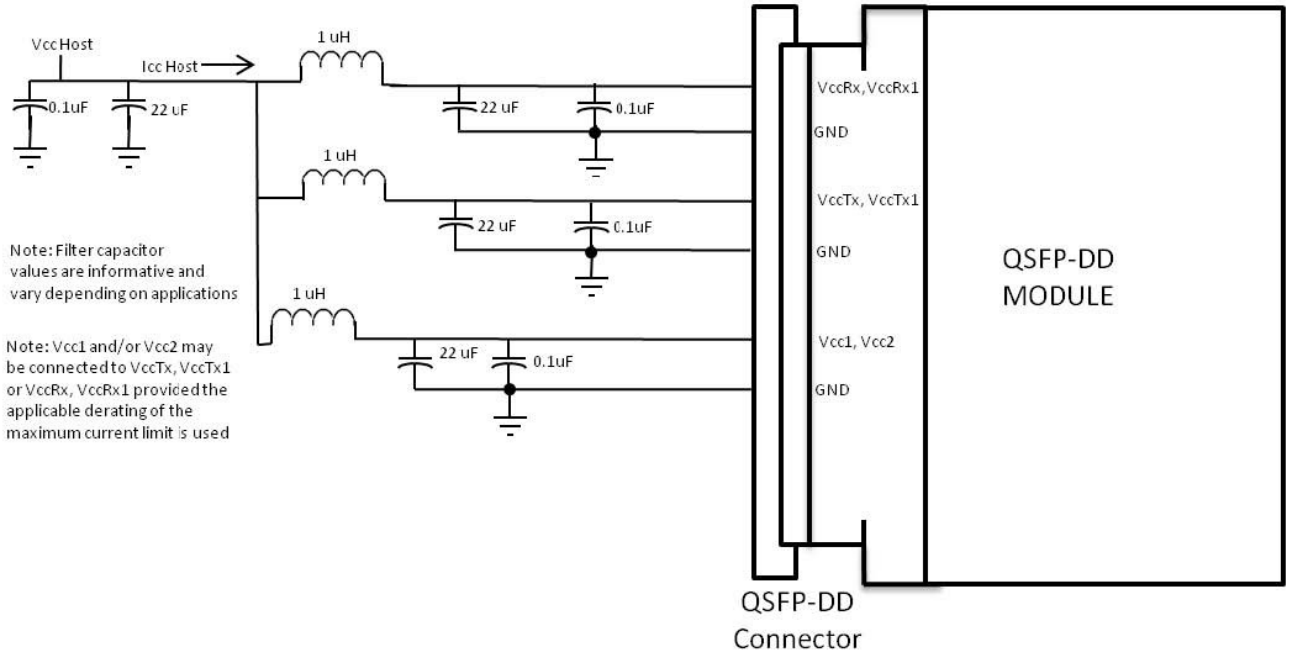
Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	
20		GND	Ground	1B	
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	
30		Vcc1	+3.3V Power supply	2B	
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	

32		GND	Ground	1B	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	

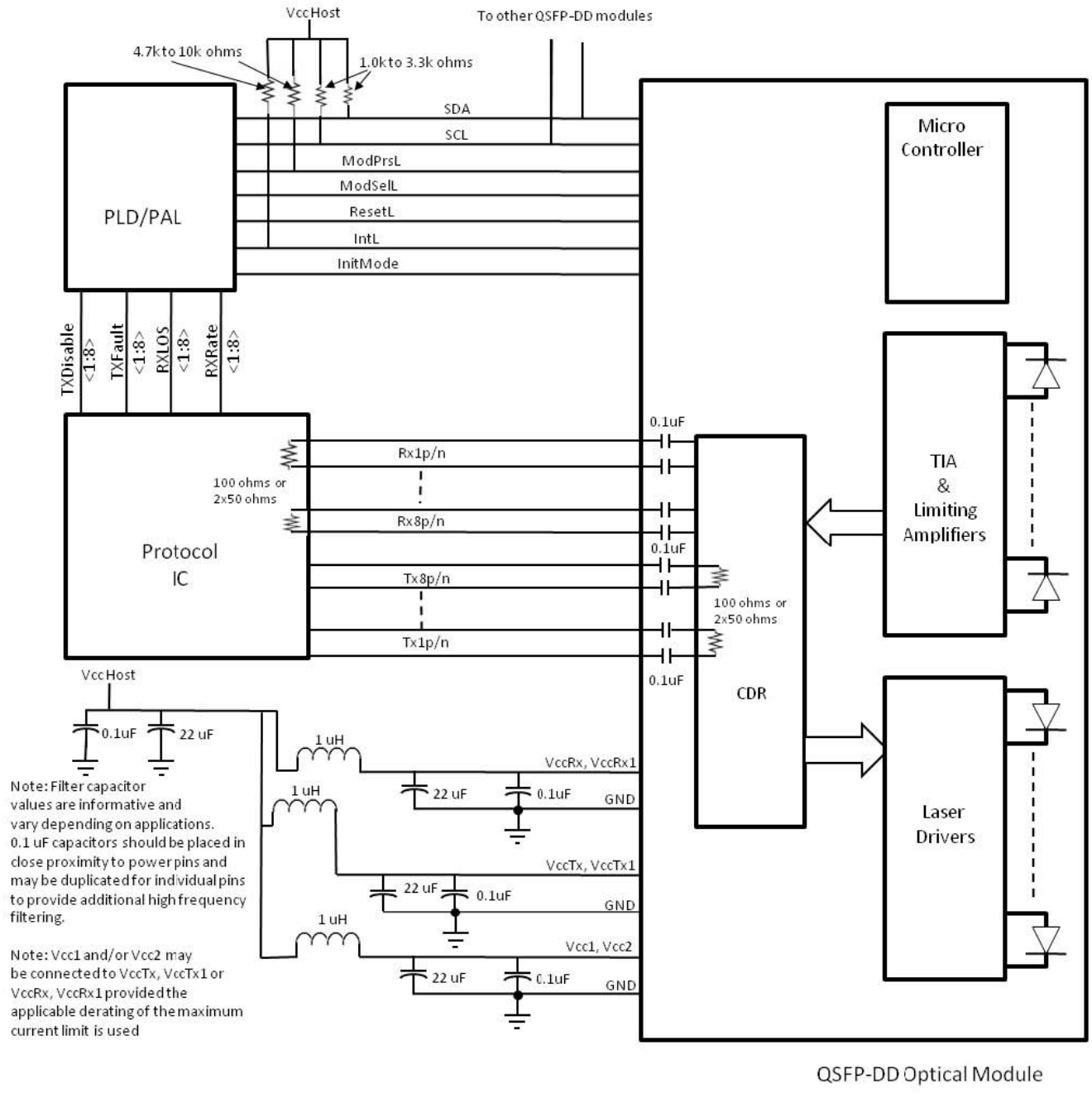
Pin	Logic	Symbol	Description	Plug Sequence	Notes
39		GND	Ground	1A	
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	
46		Reserved	For future use	3A	
47		VS1	Module Vendor Specific 1	3A	
48	VccRx1	3.3V Power Supply	2A	2	
49		VS2	Module Vendor Specific 2	3A	
50		VS3	Module Vendor Specific 3	3A	
51		GND	Ground	1A	
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	
58		GND	Ground	1A	
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	

63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	WST-QSFP+LR4L-C
64		GND	Ground	1A	
65		NC	No Connect	3A	
66		Reserved	For future use	3A	
67		VccTx1	3.3V Power Supply	2A	
68		Vcc2	3.3V Power Supply	2A	
69		Reserved	For Future Use	3A	
70		GND	Ground	1A	
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	

Recommended Host Board Power Supply Circuit

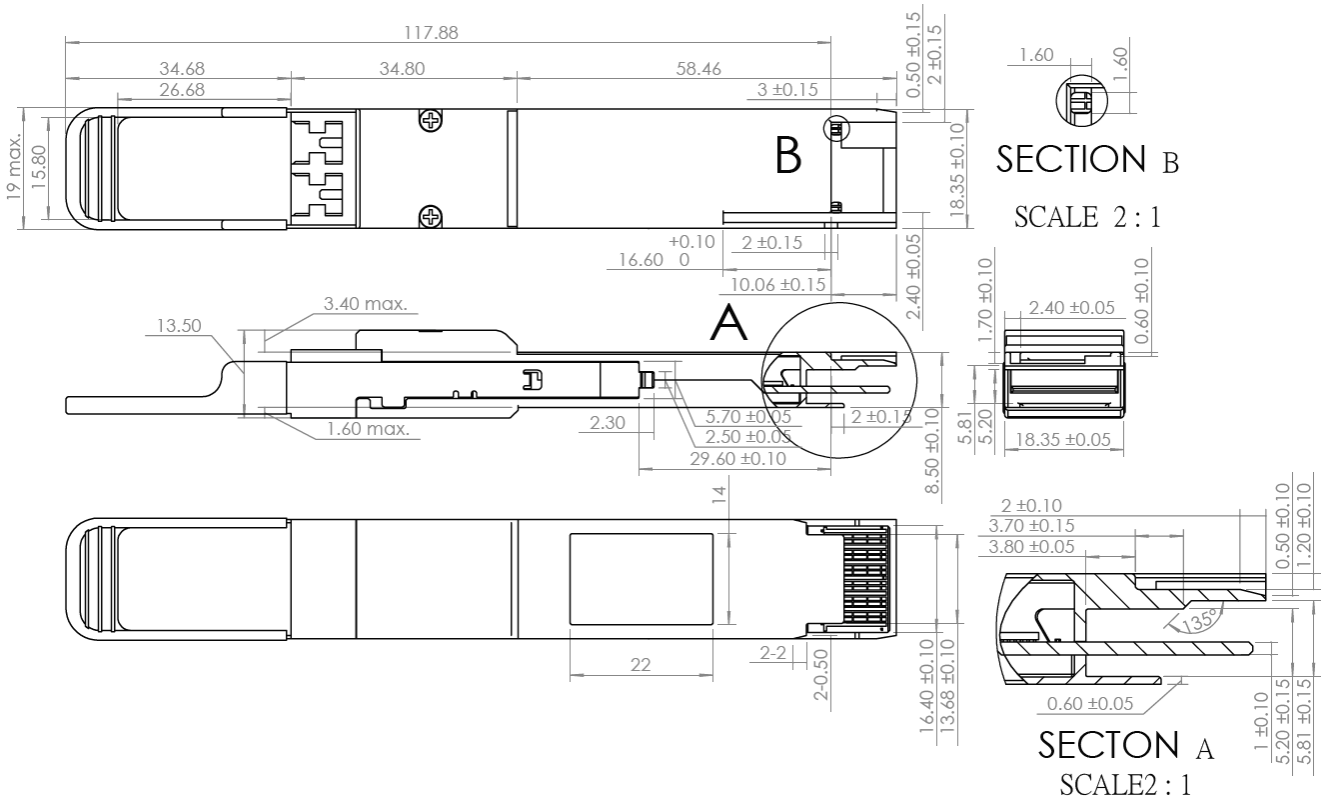


Recommended Interface Circuit



WST-QSFP+LR4L-C

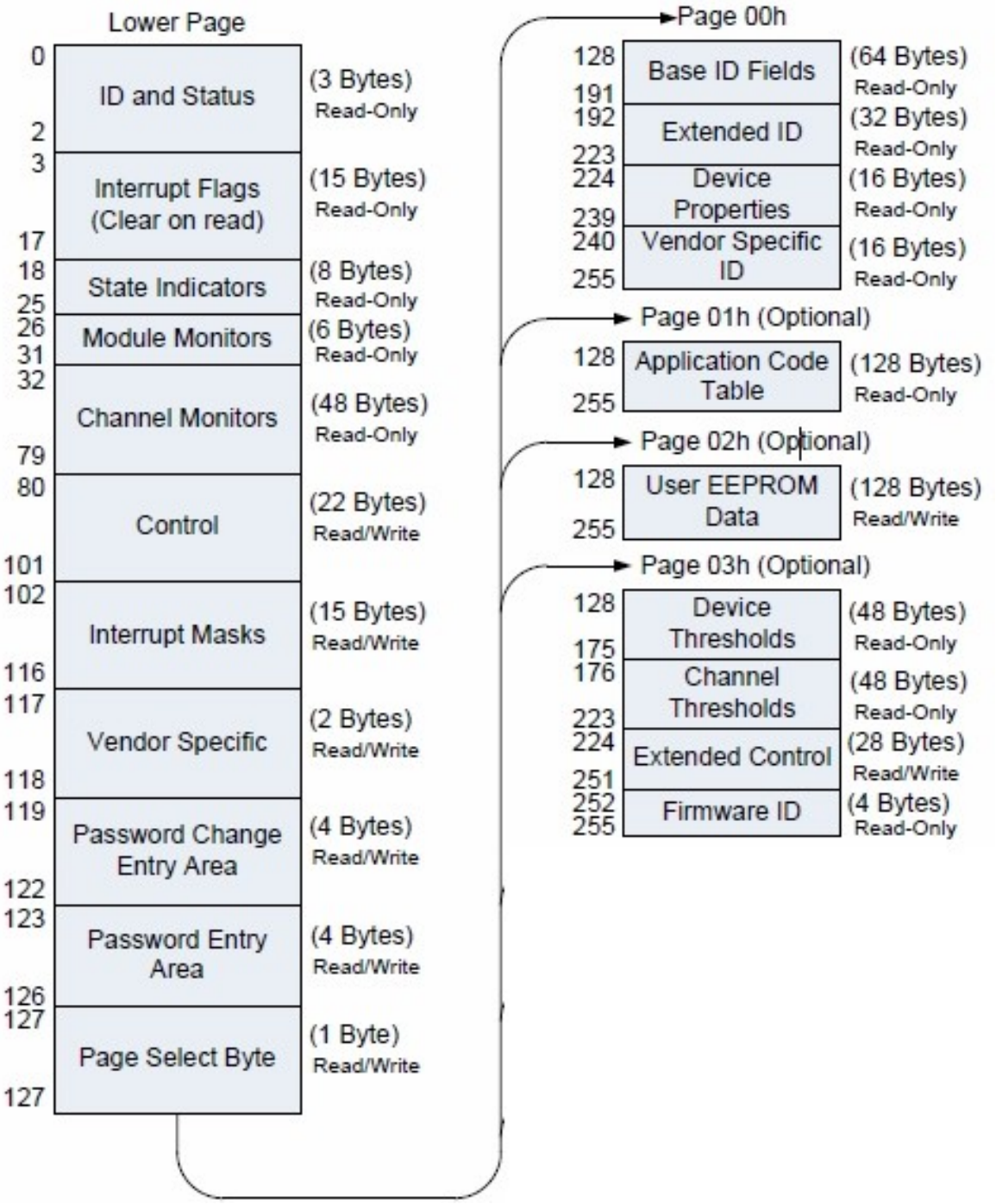
Mechanical Design Diagram



Unit: mm

Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP-DD Rev. 2.0 MSA specification as shown in the below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.



Ordering Information

Part No	Specification									
	Package	Data rate per Lane	Laser	Optical Power	Detector	Max. Receive Sensitivity (OMA)	Temp	Reach	Other	Application code
WST-QD2H-2CM4-C	QSFP-DD	25.78 Gbps each Channel	2x4 ch CWDM DML	-4.0~2.5 dBm each Channel	PIN	-10.0dBm each Channel	0~70°C	2km	DDM RoHS	200G Ethernet

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	1-Sep-2017	New release	Ivy Chen	Wayne Liao	Wayne Liao