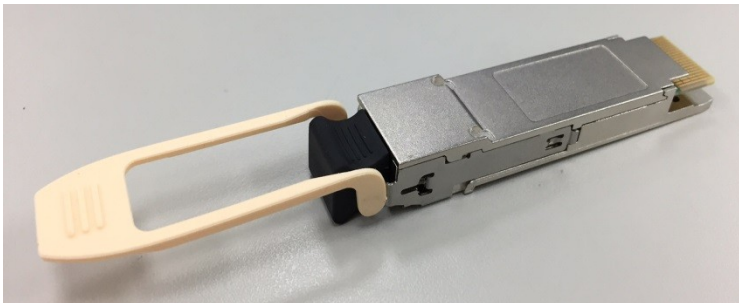
Data Sheet

200Gbps 2×SR4 QSFP-DD Optical Transceiver Module

P/N: WST-QD2H-2SR4-C



Features:

- Compliant with 100G Ethernet IEEE 802.3bm 100GBASE-SR4 standards
- Compliant to QSFP-DD Rev. 2.0
- Supports 200 Gbps data rate links of 70m/100m via OM3/OM4, respectively
- Low power consumption of max 4W (Typ. 3.5W)
- Hot pluggable electrical interface
- Using standard 2 Row by 12 Channel MPO Connector
- 0 to 70°C case temperature operating range
- RoHS-6 Compliant (lead-free)

Application:

- 2x100GBASE-SR4 Ethernet links
- HPC Interconnects
- Proprietary Interconnections

ABSOLUTE MAXIMUM RATINGS

Not necessarily applied together. Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Parameter	Min	Max	Unit	Note
Storage Temperature	-40	85	°C	
3.3V Power Supply Voltage	-0.5	3.6	V	
Data Input Voltage- Single Ended	-0.5		Vcc+0.5	
Control Input Voltage	-0.5	3.6	V	1
Relative Humidity	5	85	%	
Rx Optical Damage Threshold / Lane	3.4		dBm	

Notes:

1. Non-condensing.

Recommended Operating Conditions

Parameter	Min	Typical	Max	Unit	Note
Case Operating Temperature	0	55	70	°C	
Power Supply Voltage	3.135	3.3	3.465	V	
Date Rate per Channel		25.78125		Gbps	
Bit Error Ratio		10^{-12}			
Control Input Voltage High	2		Vcc+0.3	V	
Control Input Voltage Low	-0.3		0.8	V	
Two Wire Serial (TWS) Interface Clock Rate		100	400	kHz	
Differential Data Input / Output Load		100		Ohms	
Fiber Length: 2000 MHz·km 50/125μm MMF (OM3)	0.5		70	m	
Fiber Length: 4700 MHz·km 50/125μm MMF (OM4)	0.5		100	m	

Electrical Characteristics

Parameter	Min	Typical	Max	Unit	Note
Transceiver Electrical Characteristics					
TRx Power Consumption		3.5	4	W	
TRx Power-on Initialization Time			2000	ms	
CAUI-4 Module Electrical Input Characteristics (TP1)					
Signaling Rate per Lane		25.78125		Gbps	1
Differential pk-pk input voltage tolerance			900	mV	
Differential Input Return Loss	See Eq. 1				2
Differential to Common-mode Input Return Loss	See Eq. 2				3
Differential termination mismatch			10	%	
Module stressed input test	See Eq. 3				4
Single Ended Input Voltage Tolerance	-0.4		3.3	V	
DC common mode voltage	-350		2850	mV	

Notes:

1. Signaling rate tolerance is within +/- 100 ppm.
2. $$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases} (dB) \quad \text{(Eq.1)}$$

   where

   f is the frequency in GHz

   RLd is the CAUI-4 Chip-to-module input differential return loss

3. $$RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases} (dB) \quad \text{(Eq.2)}$$

   where

   f is the frequency in GHz

   RLdc is the CAUI-4 Chip-to-module input differential to common mode input return loss

4. The module stressed input tolerance is measured using the procedure defined in 83E.3.4.1.1, IEEE802.3bm. Module stressed input parameters include

a. Eye width of 0.46 UI

b. Applied pk-pk sinusoidal jitter is per Table 88-13 per IEEE802.3bm

c. Eye height of 95 mV

Parameter	Min	Typical	Max	Unit	Note
CAUI-4 Module Electrical Output Characteristics (TP4)					
Signaling Rate per Lane		25.78125		Gbps	1
AC Common-Mode Output Voltage (RMS)			17.5	mV	
Differential Output Voltage			900	mV	
Eye Width	0.57			UI	
Eye Height, Differential	228			mV	
Vertical Eye Closure			5.5	dB	
Differential Output Return Loss	See Eq. 1				2
Common to Differential Mode Conversion Return Loss	See Eq. 2				3
Differential termination mismatch			10	%	
Transition Time (20% to 80%)	12			ps	
DC Common Voltage	-350		2850	mV	

Notes:

1. Signaling rate tolerance is within +/- 100 ppm.

2. $$RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4\log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases} (dB) \qquad \text{(Eq.1)}$$

where

f is the frequency in GHz

RLd is the CAUI-4 Chip-to-module input differential return loss

3. $$RLdc(f) \geq \begin{cases} 22 - 20\left(\frac{f}{25.78}\right) & 0.01 \leq f < 12.89 \\ 15 - 6\left(\frac{f}{25.78}\right) & 12.89 \leq f < 19 \end{cases} (dB) \qquad \text{(Eq.2)}$$

where

f is the frequency in GHz

RLdc is the CAUI-4 Chip-to-module input differential to common mode input return loss

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit	Note
Transmitter Optical Characteristics						
Center Wavelength	λ	840		860	nm	
Spectral Width – RMS	Δλ		0.55		nm	
Average Launch Optical Power, each lane	LOP	-8.4		2.4	dBm	
Optical Modulation Amplitude, each lane	OMA	-6.4		3	dBm	
Launch power in OMA minus TDEC		–7.3			dBm	1
Transmitter and dispersion eye closure (TDEC), each lane	TDEC			4.3	dB	1
Average launch power of OFF transmitter, each lane				-30	dBm	
Extinction ratio	ER	2			dB	
Optical return loss tolerance				12	dB	
Encircled Flux		≥ 86% @ 19um, ≤ 30% at 4.5um				1
Transmitter eye mask definition		(X1, X2, X3, Y1, Y2, Y3)= (0.3, 0.38, 0.45, 0.35, 0.41, 0.5}				2

Notes:

1. Designed target and belonging to TDP for further confirmation.
2. Hit ratio 1.5×10^{-3} hits per sample

Parameter	Symbol	Min	Typical	Max	Unit	Note
Receiver Optical Characteristics						
Center wavelength, each lane	λ	840		860	nm	
Damage Threshold		3.4			dBm	
Average power at receiver input, each lane		-10.3		2.4	dBm	1
Receive Power, each lane (OMA)				3	dBm	
Receiver Reflectance				-12	dB	
Stressed receiver sensitivity in OMA				-5.2	dBm	
Conditions of stressed receiver sensitivity test:						
Stressed eye closure (SEC)			4.3		dB	2
Stressed eye J2 Jitter			0.39		UI	2
Stressed eye J4 Jitter,				0.53	UI	2
OMA of each aggressor lane				3	dBm	2
Stressed receiver eye mask definition		(X1, X2, X3, Y1, Y2, Y3)= (0.28, 0.5, 0.5, 0.33, 0.33, 0.4}				3

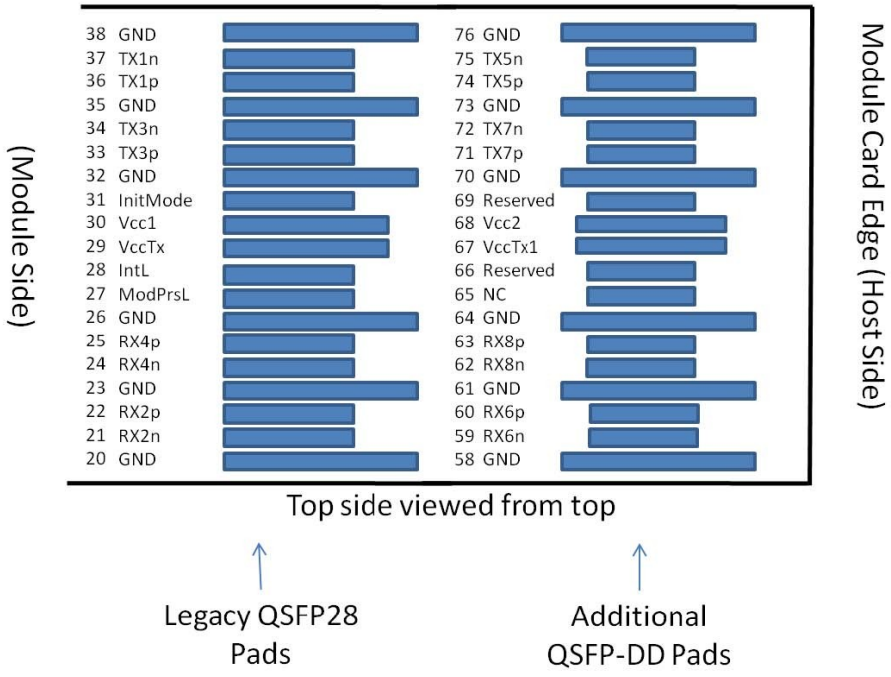
Notes:

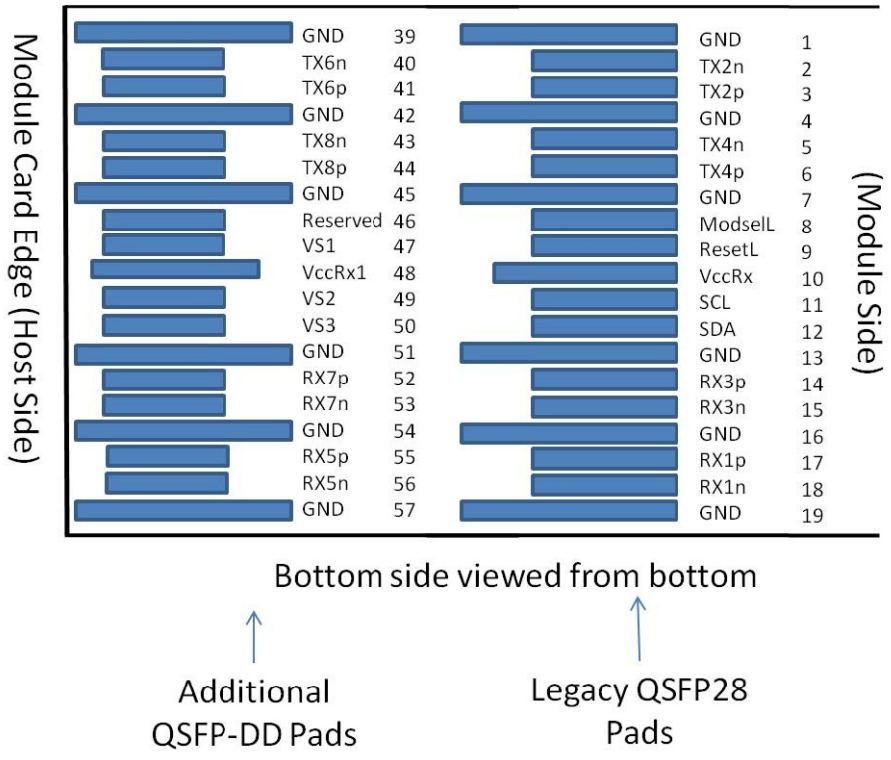
1. Average receive power, each lane (min) is informative and not the principal indicator of signal strength. A received power below this value cannot be compliant; however, a value above this does not ensure compliance.

2. TDP value and dependent parameters are subject to confirmation.

3. Hit ratio 5×10^{-5} hits per sample

QSFP28 Module Pad Assignments and Descriptions



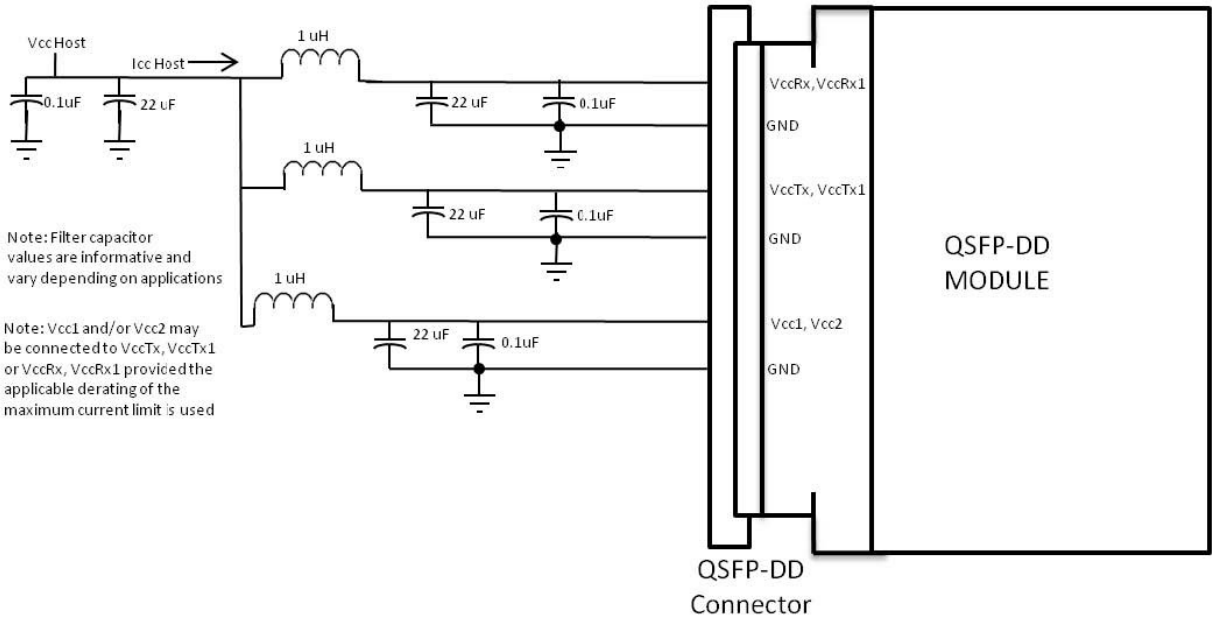


Pin	Logic	Symbol	Description	Plug Sequence	Notes
1		GND	Ground	1B	
2	CML-I	Tx2n	Transmitter Inverted Data Input	3B	
3	CML-I	Tx2p	Transmitter Non-Inverted Data Input	3B	
4		GND	Ground	1B	
5	CML-I	Tx4n	Transmitter Inverted Data Input	3B	
6	CML-I	Tx4p	Transmitter Non-Inverted Data Input	3B	
7		GND	Ground	1B	
8	LVTTL-I	ModSelL	Module Select	3B	
9	LVTTL-I	ResetL	Module Reset	3B	
10		VccRx	+3.3V Power Supply Receiver	2B	
11	LVCMOS-I/O	SCL	2-wire serial interface clock	3B	
12	LVCMOS-I/O	SDA	2-wire serial interface data	3B	
13		GND	Ground	1B	
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	3B	
15	CML-O	Rx3n	Receiver Inverted Data Output	3B	
16		GND	Ground	1B	
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	3B	
18	CML-O	Rx1n	Receiver Inverted Data Output	3B	
19		GND	Ground	1B	
20		GND	Ground	1B	
21	CML-O	Rx2n	Receiver Inverted Data Output	3B	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	3B	
23		GND	Ground	1B	
24	CML-O	Rx4n	Receiver Inverted Data Output	3B	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	3B	
26		GND	Ground	1B	
27	LVTTL-O	ModPrsL	Module Present	3B	
28	LVTTL-O	IntL	Interrupt	3B	
29		VccTx	+3.3V Power supply transmitter	2B	
30		Vcc1	+3.3V Power supply	2B	
31	LVTTL-I	InitMode	Initialization mode; In legacy QSFP applications, the InitMode pad is called LPMODE	3B	

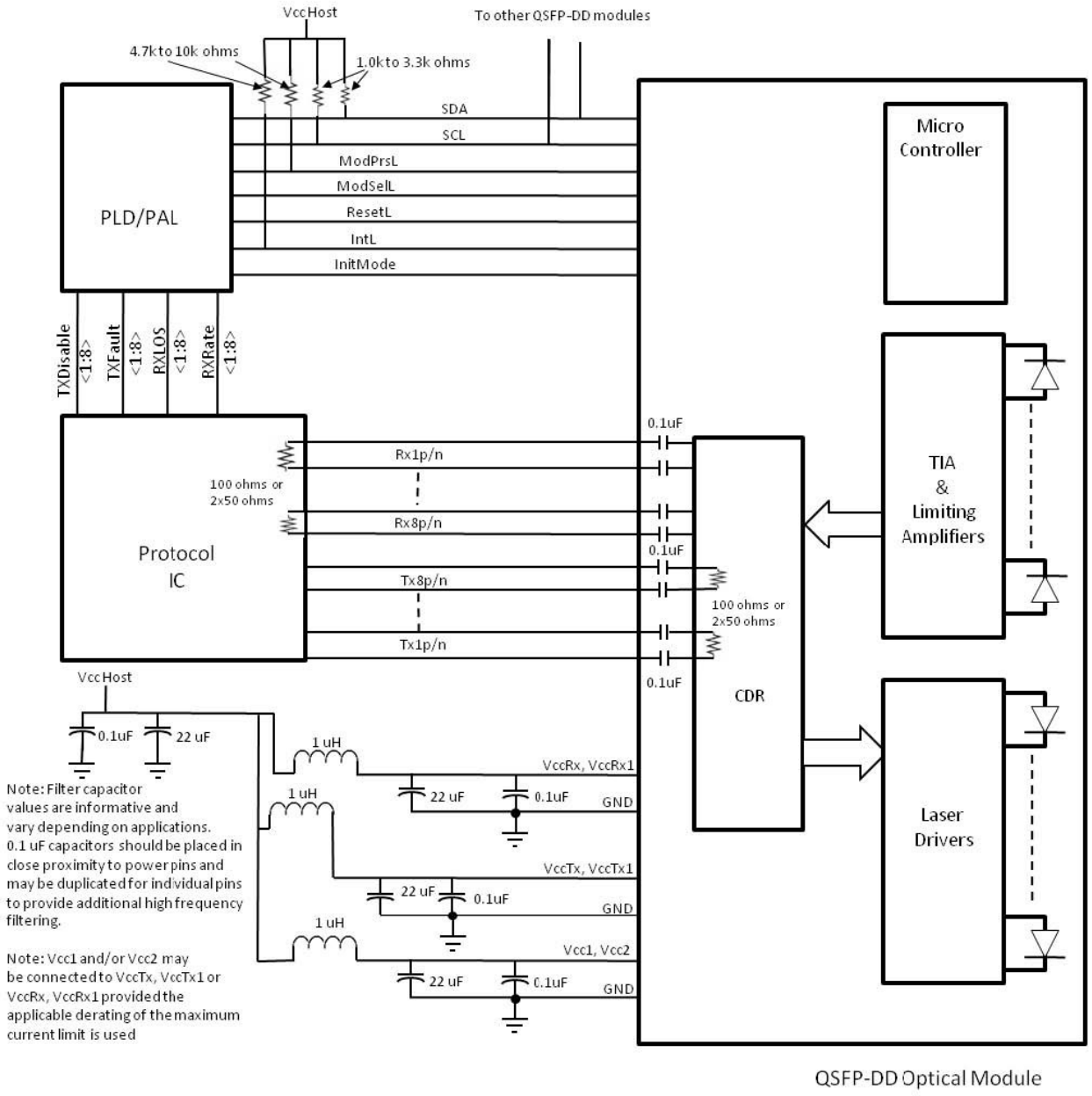
32		GND	Ground	1B	
33	CML-I	Tx3p	Transmitter Non-Inverted Data Input	3B	
Pin	**Logic**	**Symbol**	**Description**	**Plug Sequence**	**Notes**
34	CML-I	Tx3n	Transmitter Inverted Data Input	3B	
35		GND	Ground	1B	
36	CML-I	Tx1p	Transmitter Non-Inverted Data Input	3B	
37	CML-I	Tx1n	Transmitter Inverted Data Input	3B	
38		GND	Ground	1B	
39		GND	Ground	1A	
40	CML-I	Tx6n	Transmitter Inverted Data Input	3A	
41	CML-I	Tx6p	Transmitter Non-Inverted Data Input	3A	
42		GND	Ground	1A	
43	CML-I	Tx8n	Transmitter Inverted Data Input	3A	
44	CML-I	Tx8p	Transmitter Non-Inverted Data Input	3A	
45		GND	Ground	1A	
46		Reserved	For future use	3A	
47		VS1	Module Vendor Specific 1	3A	
48	VccRx1	3.3V Power Supply	2A	2	
49		VS2	Module Vendor Specific 2	3A	
50		VS3	Module Vendor Specific 3	3A	
51		GND	Ground	1A	
52	CML-O	Rx7p	Receiver Non-Inverted Data Output	3A	
53	CML-O	Rx7n	Receiver Inverted Data Output	3A	
54		GND	Ground	1A	
55	CML-O	Rx5p	Receiver Non-Inverted Data Output	3A	
56	CML-O	Rx5n	Receiver Inverted Data Output	3A	
57		GND	Ground	1A	
58		GND	Ground	1A	
59	CML-O	Rx6n	Receiver Inverted Data Output	3A	
60	CML-O	Rx6p	Receiver Non-Inverted Data Output	3A	
61		GND	Ground	1A	
62	CML-O	Rx8n	Receiver Inverted Data Output	3A	

63	CML-O	Rx8p	Receiver Non-Inverted Data Output	3A	
64		GND	Ground	1A	
65		NC	No Connect	3A	
66		Reserved	For future use	3A	
Pin	**Logic**	**Symbol**	**Description**	**Plug Sequence**	**Notes**
67		VccTx1	3.3V Power Supply	2A	
68		Vcc2	3.3V Power Supply	2A	
69		Reserved	For Future Use	3A	
70		GND	Ground	1A	
71	CML-I	Tx7p	Transmitter Non-Inverted Data Input	3A	
72	CML-I	Tx7n	Transmitter Inverted Data Input	3A	
73		GND	Ground	1A	
74	CML-I	Tx5p	Transmitter Non-Inverted Data Input	3A	
75	CML-I	Tx5n	Transmitter Inverted Data Input	3A	
76		GND	Ground	1A	

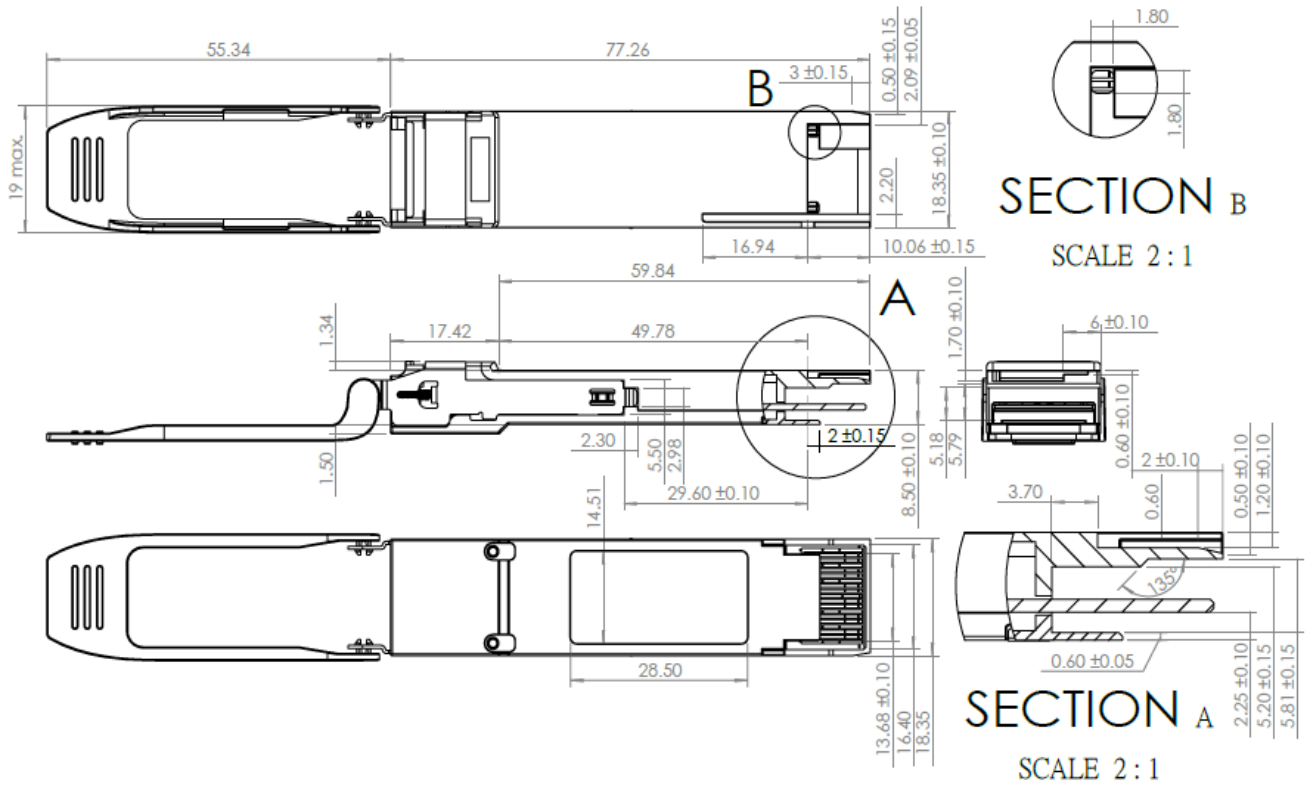
Recommended Host Board Power Supply Circuit



Recommended Interface Circuit



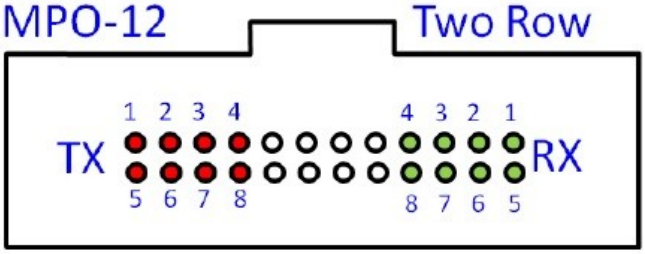
Mechanical drawing



Unit: mm

Optical-Channel Definition for 2 Row 12C Fiber

Optical-Channel Definition for 2 Row 12C Fiber

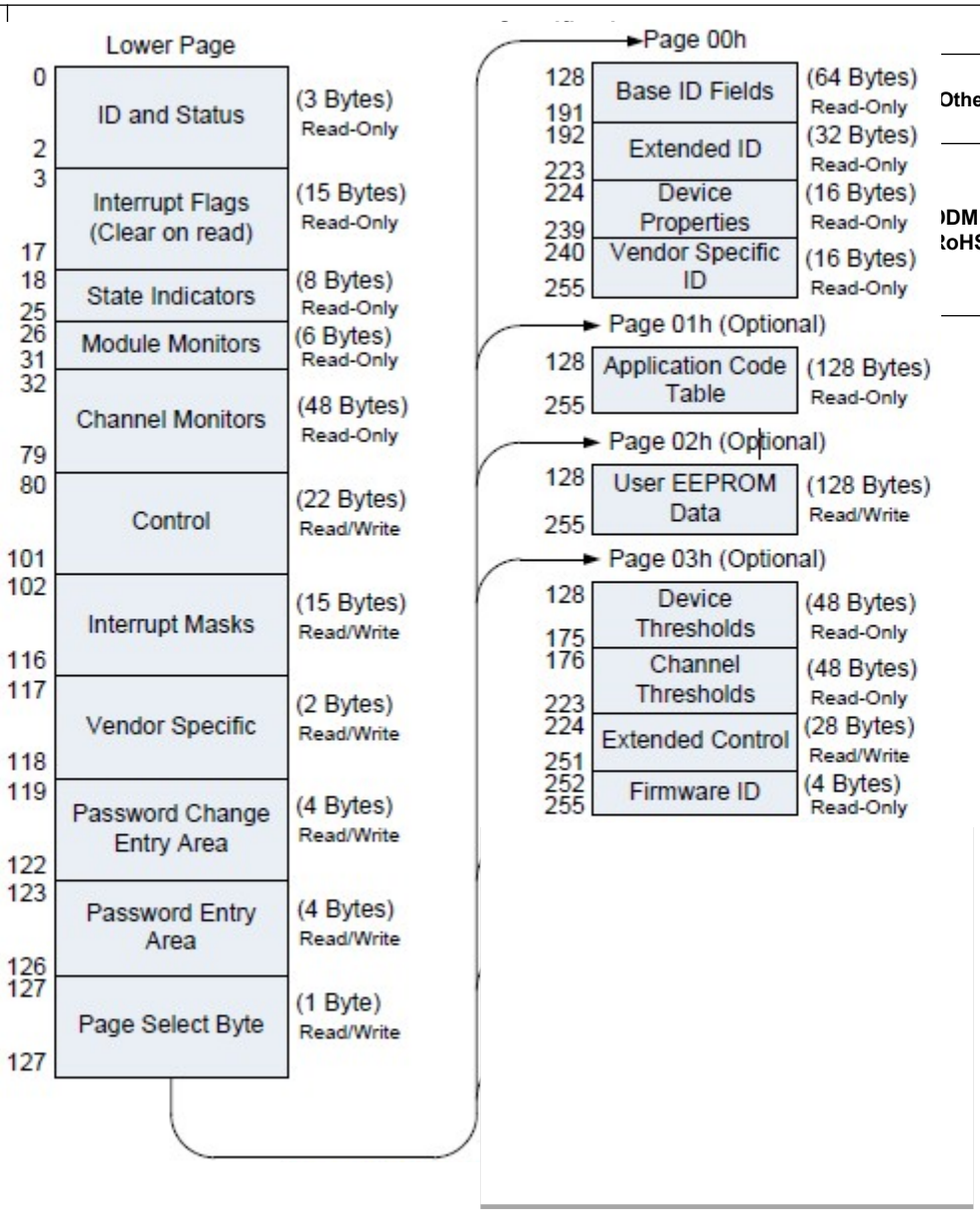


Memory Map

The memory map is structured as a single address and multiple page approaches, according to the QSFP DD rev.2.0 specification as shown in the below. For more detailed description of this memory map or lower pages, please see our Memory Map document with flexible customization settings.

Order information

Part No	Other	Application code
WST-QD2H-2SR4-C	DDM RoHS	200G Ethernet



Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	13-Sep-17	New Issue	Ivy Chen	Wayne Liao	Wayne Liao
V1.1	7-Nov-17	Picture change	Ivy Chen	Wayne Liao	Wayne Liao

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