

200G QSFP56 SR4 100m Transceiver Module

P/N: WST-QS56-SR4-C



Features:

- Hot Pluggable QSFP form factor
- Supports 212.5Gb/s aggregate bit rate
- Low Power Dissipation, Typ. 5.0W
- Up to 70m transmission with OM3 multi-mode fiber and 100m transmission with OM4 multi-mode fiber.
- 4x50G PAM4 VCSEL/PIN photo detector
- Operating Case Temperature: 0°C~70
- SFF-8636 Management Interface
- SFF-8679: General Electrical
- IEEE 802.3cd: Physical Layer Specifications and Management Parameters
- ROHS-6: Environment Safety

Applications:

- Ethernet for 200GBASE-SR4

General Product Characteristic

Parameter	Value	Unit	Comments
Module Form Factor	QSFP	As defined by SFF-8661	Module Form Factor
Number of Lanes	4 TX and 4 RX		
Maximum Aggregate Data Rate	212.5	Gb/s	
Protocols Supported	Ethernet		
Electrical Interface and Pin-out	38-pin edge connector		Pin-out as defined by SFF-8679
Maximum Power Consumption per End	5	Watts	Varies with output voltage swing and pre-emphasis settings
Management Interface	Serial, I2C-based, 400 kHz maximum frequency		As defined by SFF-8636

Absolute Maximum Ratings

Exceeding the limits below may damage the optical transceiver module permanently.

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Maximum Supply Voltage	V_{cc}	-0.5		3.6	V	
Storage Temperature	T_{sto}	-40		85	°C	
Case Operating Temperature	T_{op}	0		70	°C	
Relative Humidity	RH	0		85	%	1

Notes:

1. No-condensing.

Parameters

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Supply Voltage	V_{cc}	3.14		3.46	V	
Power Consumption	P_{Con}		5		W	
Bit Rate	BR		26.5625		GBd	1
Bit Error Ratio	BER	10^{-6}				2
Center wavelength	λ_c	840		860	nm	3
Number of Lanes		4				
Management Interface		Serial, I2C-based, maximum frequency 400 kHz				4
Logic Input Voltage High	V_{ih}	2		$V_{cc}+0.3$	V	
Logic Input Voltage Low	V_{il}	-0.3		0.8	V	

Notes:

1. Single lane
2. PRBS13Q test pattern is used.
3. As defined by IEEE Std. 802.3cd™/D2.1
4. As defined by SFF-8636

Electrical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Transceiver Power Supply Current	I_{cc}		1600		mA	
Transceiver Power On Initialization Time	T_{init}			2000	ms	
Transmitter at TP1a						
AC common-mode output voltage (RMS)				17.5	mV	
Differential peak-to-peak output voltage (Transmitter disabled)				35	mV	
Differential peak-to-peak output voltage (Transmitter enabled)				880	mV	
Eye symmetry mask width	ESMW		0.22		UI	
Eye height, differential	EH	32			mV	
Differential output return loss		See Eq. 1				
Common to differential mode conversion return loss		See Eq. 2				
Differential termination mismatch		10			%	
Transition time (20% to 80%)	T_r, T_f	10			ps	
Receiver at TP4						
Far-end Eye height, differential		30			mV	
Far-end pre-cursor ISI ratio		-4.5		2.5	%	
Differential output return loss		See Eq. 1				
Common to differential mode conversion return loss		See Eq. 2				
Differential termination mismatch		10			%	
Transition time (20% to 80%)	T_r, T_f	10			ps	
DC common mode voltage		-350		2850	mV	

Notes:

$$1. \quad RLd(f) \geq \begin{cases} 9.5 - 0.37f & 0.01 \leq f < 8 \\ 4.75 - 7.4 \log_{10}\left(\frac{f}{14}\right) & 8 \leq f < 19 \end{cases} (dB) \quad (Eq.1)$$

where

 f is the frequency in GHz, RLd is the CAUI-4 Chip-to-module input differential return loss

$$2. \quad RL_{dc}(f) \geq \begin{cases} 22 - 20 \left(\frac{f}{25.78} \right) & 0.01 \leq f < 12.89 \\ 15 - 6 \left(\frac{f}{25.78} \right) & 12.89 \leq f < 19 \end{cases} \quad (dB) \quad (Eq.2)$$

where

f is the frequency in GHz,

RL_{dc} is the CAUI-4 Chip-to-module input differential to common mode input return loss

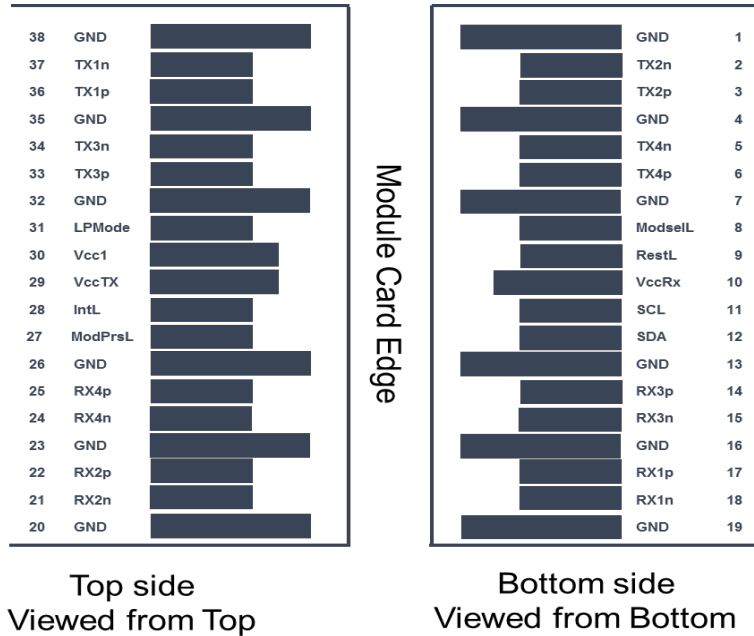
Optical Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit.	Ref.
Transmitter						
Signaling Speed per Lane		26.5625 ± 100 ppm			GBd	
Lane wavelengths (Range)	λ	840		860	nm	
RMS Spectral Width	$\Delta\lambda$			0.6	nm	
Average launch power, each lane	P_{avg}	-6		4	dBm	
Outer Optical Modulation Amplitude (OMA _{outer}), each lane (max)		-4		3	dBm	
Transmit OMA per Lane	OMA	-6.4		3	dBm	
Transmitter and dispersion eye closure (TDEC), each lane	TDEC			4.9	dBm	
Launch power in OMA _{outer} minus TDECQ (min)		-5.9			dBm	
Extinction ratio	ER	3			dB	
Average launch power of OFF transmitter, each lane	P_{off}			-30	dBm	
Receiver						
Signaling Speed per Lane		26.5625 ± 100 ppm			Gb/s	
Lane wavelengths (Range)	λ	840		860	nm	
Damage threshold		+5			dBm	
Average power at receiver input, each lane		-7.9		4	dBm	1
Receive Power, each lane (OMA)				3	dBm	
Receiver Reflectance				-12	dB	
Receiver sensitivity in OMA _{outer}				-7.0	dBm	2

Notes:

1. Average receive power, each lane (min) is informative and not the principal indicator of signal strength.
2. Receiver sensitivity is informative and is defined for a transmitter with SECQ = 0.9 dB.

Pin Assignment



PIN	Symbol	Description	Ref.
1	GND	Ground	
2	TX2n	Transmitter Inverted Data Input	
3	TX2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	TX4n	Transmitter Inverted Data Input	
6	TX4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	2
9	ResetL	Module Reset	2
10	V _{cc} RX	+3.3V Receiver Power Supply Receiver	
11	SCL	2-wire Serial Interface Clock	2
12	SDA	2-wire Serial Interface Data	2
13	GND	Ground	1

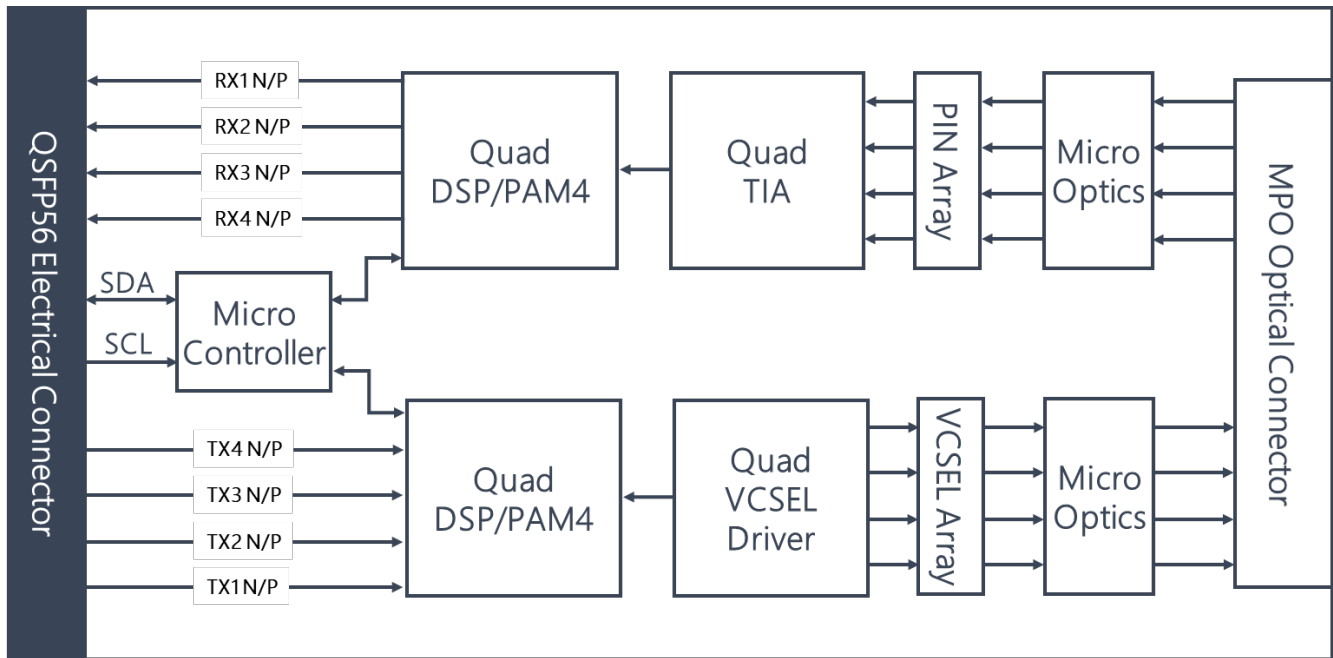
14	RX3p	Receiver Non-Inverted Data Output	
15	RX3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	RX1p	Receiver Non-Inverted Data Output	
18	RX1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	RX2n	Receiver Inverted Data Output	
22	RX2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	RX4n	Receiver Inverted Data Output	
25	RX4p	Receiver Non-Inverted Data Output	
26	GND	Ground	1
27	ModPrsL	Module Present, internal pulled down to GND	
28	IntL	Interrupt output, should be pulled up on host board	
29	Vcc TX	+3.3V Transmitter Power Supply	
30	Vcc1	+3.3V Power Supply	
31	LPMODE	Low Power Mode	2
32	GND	Ground	
33	TX3p	Transmitter Non-Inverted Data Input	
34	TX3n	Transmitter Inverted Data Input	
35	GND	Ground	
36	TX1p	Transmitter Non-Inverted Data Input	
37	TX1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes:

1. GND is the symbol for signal and supply (power) common for the module. All are common within the module and all module voltages are reference to this potential unless otherwise noted. Module circuit ground is isolated from module chassis ground within the module.
2. Open collector, should be pulled up with 4.7~10K ohms on the host board to a voltage between 3.15V

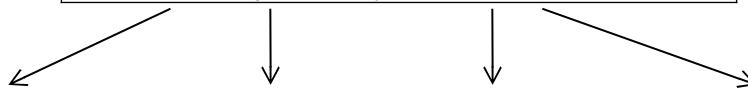
and 3.6V.

Recommended Host Board Schematic



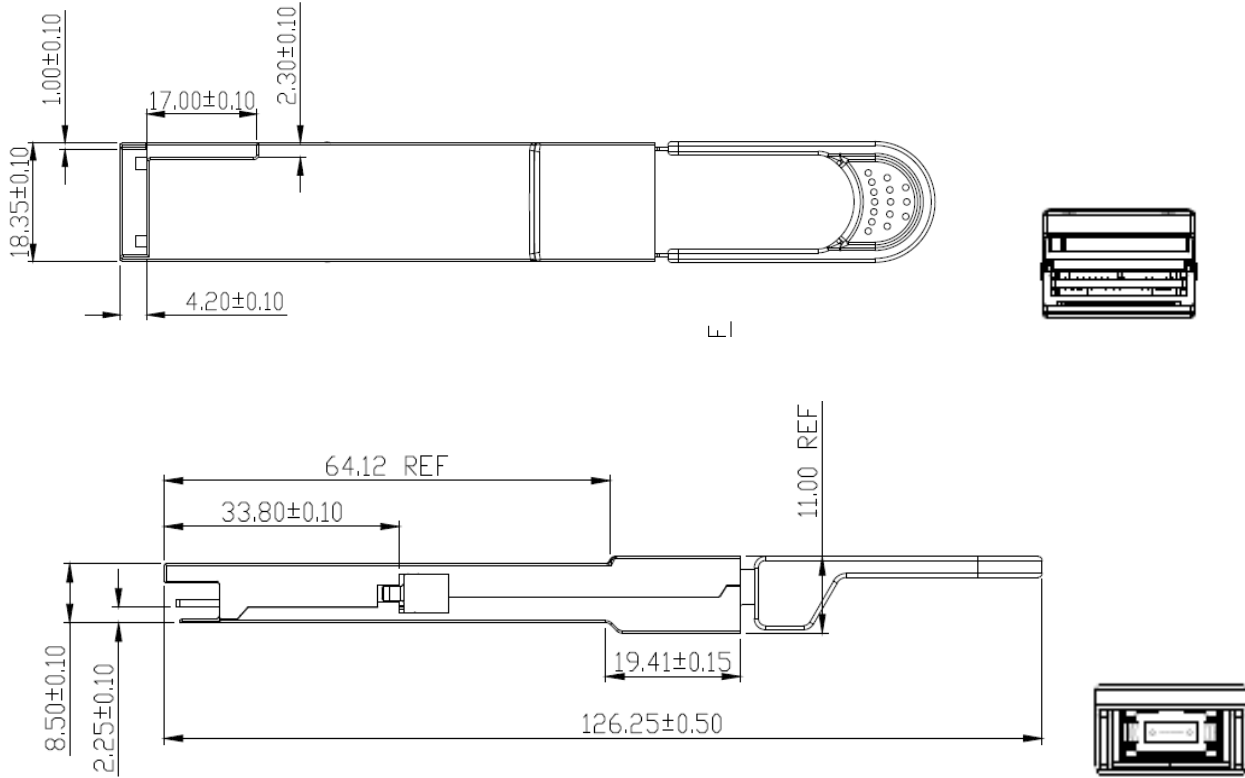
Memory Map (compliant SFF-8636)

	2-Wire Serial Address 1010000x
	Lower Page 00h
0	Identifier
1-2	Status
3-21	Interrupt Flags
22-23	Free Side Device Monitors
34-81	Channel Monitors
82-85	Reserved
86-98	Control
99	Reserved
100-104	Hardware Interrupt Pin Masks
105-106	Vendor Specific
107	Reserved
108-110	Free Side Device Properties
111-112	Assigned for use by PCI Express
113	Free Side Device Properties
114-118	Reserved
119-122	Password Change Entry Area (Optional)
123-126	Password Entry Area (Optional)
127	Page Select Byte



	Optional	Optional	Optional
Upper Page 00h	Page 01h	Page 02h	Page 03h
128 Identifier	128 CC_APPS	128-255 User EEPROM data	128-175 Free Side Device Thresholds
129-191 Base ID Fields	129 AST Table Length (TL)		
	130-131 Application Code Entry 0		
	132-133 Application Code Entry 1		
	134-253 other entries		
192-223 Extended ID			176-223 Channel Thresholds
224-255 Vendor Specific ID			224 TX EQ & RX Emphasis Magnitude ID
			225 RX output amplitude indicators
			226-241 Channel Monitor Masks
	254-255 Application Code Entry TL		252-255 Reserved

Mechanical Drawing



Unit: mm

Ordering Information

Part No	Specification									
	Package	Data rate per Lane	Laser	Optical Power	Detector	Max. Receive Sensitivity (OMA)	Temp	Reach	Other	Application code
WST-QS56-SR4-C	QSFP56	26.5625 GBd per channel	4x50G PAM4 VCSEL	-6~ +4 each Channel	PIN	-7.0 dBm each Channel	0~70°C	70m via OM3; 100m via OM4	DDM RoHS	200GBASE-SR4

Modification History

Revision	Date	Description	Originator	Review	Approved
V1.0	15-Jun-2020	New Issue	Ivy Chen	Wayne Liao	Wayne Liao

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